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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/832,167	04/09/2001	Yusuke Tsutsui	81784.0235	8829

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EXAMINER	
KUMAR, SRILAKSHMI K	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,167	TSUTSUI ET AL.	
	Examiner	Art Unit	
	Srilakshmi K. Kumar	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The following office action is in response to the Request for Continued Examination, filed February 7, 2005. Claims 45-50 are newly added. Claims 1-50 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 8-14, 16-23, 25-27, 29, 32-35, 37, and 40-50 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki (US 2002/0175887 A1).

As pertaining to claims 1, 11 and 20, Yamazaki teaches an LCD in which is comprised of a plurality of pixels in a matrix having n rows and m columns (fig. 1). As figure 1 depicts, there are a total of 200 row lines for a normal or full display, then the display when needed is able to divide itself into a partial display of s rows, which are 40 rows, and a background display or non-display of k rows, which are 160 rows. Also, figure 1 depicts n, m, s and k to be integers greater than 1 and s<n and k<n. Furthermore, Yamazaki teaches two different driving methods for writing data into the partial and non-display regions frame by frame and into each active pixel. One method is MLS, multi-line scanning method, in which a group of lines are scanned (paragraph 31; 36; 167-168). The group can range from 2-7 lines. The second method is SA, smart addressing method, in which the lines are scanned one by one or it can be construed as a sequential scan method (paragraphs 31, 188-200).

As pertaining to independent claims 27, 35 and 42 Yamazaki discloses a drive circuit for a LCD of a plurality of pixels in a matrix having n rows and m columns (fig. 1, 15). As figure 1 depicts there are a total of 200 row lines for a normal display or full display, then the display when needed is able to divide itself into a partial display of s rows, which are 40 rows, and a background display or non-display of k rows, which are 160 rows. Also, figure 1 depicts n, m, s and k to be integers greater than 1 and s < n and k < n. Furthermore, Yamazaki teaches two different driving method for writing data into the partial and non-display regions frame by frame. One method is IVILS, multi-line scanning method, in which a group of lines are scanned (paragraphs 31; 36; 167-168). The group can range from 2-7 lines. The second method is SA, smart addressing method, in which the lines are scanned one by one or it can be construed as a sequential scan method (paragraphs 31, 188-200). Furthermore, figure 15 depicts a block 2 represents a Y driver that selectively applies the selection voltages or the non-selection voltages to the plural scanning electrodes. A block 3 represents an X driver that applies the signal voltages (ON voltages, OFF voltages, and intermediate voltages there between when necessary) according to the display data Dn to the signal electrodes. A driving-voltage forming circuit represented by a block 4 forms plural voltage levels necessary for driving the liquid crystal, and the plural voltage levels formed therein are fed to the X driver 3 or the Y driver 2. From the fed voltage levels, the respective drivers selects predetermined voltage levels in accordance with timing signals and display data and apply the selected voltage levels to the signal voltages and the scanning electrodes of the liquid crystal display panel 1. A block 5 represents an LCD controller that forms timing signals CLY, FIRM, CLX, and LP, display data Dn, and a control signal PD which are necessary for the foregoing circuits and that is connected to a system bus of

an electronic equipment including this liquid crystal display apparatus. A block 6 represents a power source arranged outside of the liquid crystal display apparatus to feed power to the liquid crystal display apparatus (paragraph 239). CLY can be construed as a row clock generator because it would correspond to a row selection duration of each row, and it would be inherent a counter is established in the controller because it would allow the counting of a row clock during one frame. Furthermore, Y driver 2 and X driver 3 would have some sort of partial and background detector for detecting a signal that would initialize the display to start as a full-screen or normal display then transform itself to a partial screen display and background or non-display. Then drive voltage forming circuit 4 in conjunction with X driver and Y driver would produce a drive signal corresponding the a partial display data or background display data.

As pertaining to claims 2, 12 and 21, Yamazaki teaches the display device the row to be selected associated with pixels of area of k rows by m columns in background area is shifted every one frame (paragraphs 54-55, 158-159, 169, 188-200). Claims 2, 12 and 21 are dependent on claims 1, 11 and 20, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 3, 13, 22, Yamazaki teaches the background or non-display region over a total frame duration (paragraphs; 158-159, 188-200). Claims 3, 13 and 22 are dependent on claims 1-2, 11-12, and 20-21, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 4 and 14, Yamazaki teaches the background or non-display data is written into each pixel in the background or non-display region over a total frame duration (paragraphs; 158-159; 188-200). Also, the polarities of the background display data are inverted with respect to reference potential and inverted background display data is written into pixels in

the same row over a next total frame duration (paragraphs 38, 148,165, 195). Claims 4 and 14 are dependent on claims 1-2 and 11-12, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 5 and 23 Yamazaki discloses writing data to the partial and background regions via two methods: one method is MILS, multi-line scanning method, in which a group of lines are scanned (paragraphs 31; 36; 167168). The group can range from 2-7 lines; the second method is SA, smart addressing method, in which the lines are scanned one by one or it can be construed as a sequential scan method (paragraphs 31, 188200). Implicitly, Yamazaki discloses that if the certain rows of k are selected to be written that the other rows or remaining rows of k would not be selected to be written because they are not used for writing in that instance in which the section of rows are being used for displaying. Claims 5 and 23 are dependent on claims 1 and 20-21, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 8 and 16 Yamazaki teaches the background display data is written to all of the pixels on the matrix of n rows and m columns after a partial display instruction has been issued, then the partial display data is sequentially written into pixels of partial area of s rows and m columns and background display data is written into pixels of k rows and m columns (paragraphs 31; 36; 167-168 and 188-200). Claims 8 and 16 are dependent on claims 1 and 11, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 9, 18 and 25, Yamazaki teaches the background display data comprised off-display or arbitrary background color data (paragraph 51). Claims 9, 18, and 25

are dependent on claims 1, 11 and 20, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 10, 19 and 26, Yamazaki teaches the display device is a liquid crystal device (title; paragraph 1). Claims 10, 19 and 26 are dependent on claims 1, 11, and 20, respectively and are rejected on the same basis and what is stated above.

As pertaining to claim 17, Yamazaki teaches the during the next frame (after the first frame) and the following frames (after the second frame), the partial display instruction is detected, the partial display data is sequentially written into each pixel of the partial display region of s rows by m columns and the background display data is sequentially written into each pixel of k rows by m columns (paragraphs 31, 36, 54-55, 158-159, 167-169, 188-200). Claim 17 is dependent on claims 11 and 16 and is rejected on the same basis and what is stated above.
As pertaining to claim 32, Yamazaki teaches a mode changeover timing controller for changing from a normal display to a partial display and changing all of the data from the matrix of n rows by m columns to the background display in a next frame. The driver control signal generator would start to generate drive signals for the next frame (paragraphs 31; 36; 167-168 and 188-200). Claim 32 is dependent on claim 27 and is rejected on the same basis and what is stated above.

As pertaining to claims 29 and 37, Yamazaki teaches a polarity inverted signal generator for inverting a polarity of display data with respect to a predetermined reference voltage every unit duration or frame and the pixels in the background area selected once over one background display duration and the polarity inverted signal generator detects an arrival of the next one background duration or frame and inverts the polarity of the background data (paragraphs 38,

148,165, 195). Claims 29 and 37 are dependent on claims 27 and 35, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 33, 40, and 43, Yamazaki teaches the background display data comprised off-display or arbitrary background color data (paragraph 51). Claims 33, 40 and 43 are dependent on claims 27, 35 and 42, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 34, 41, and 44, Yamazaki teaches the display device is a liquid crystal device (title; paragraph 1). Claims 34, 41 and 44 are dependent on claims 27, 35 and 42, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 45-50, Yamazaki teaches in Fig. 23, and paragraphs 0254-0255, where the active matrix type liquid crystal display panel (item 1) is structured such that a switching device formed of a transistor is formed for each pixel in the vicinity of where the scanning electrode and the signal electrode cross each other. As well known, a gate of the transistor arranged for each pixel for each pixel is connected to the scanning electrode, a source is connected to the signal electrode, and a drain is connected to the pixel electrode. The are allowed to be conductive each other according to the selection voltage applied to in a selection period, and the feed a data signal to the pixel electrode through the transistor.

Claim Rejections - 35 USC § 103

3. Claims 6, 7, 15, 24, 30, 31, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki.

As pertaining to claims 6, 15 and 24, Yamazaki discloses a partial display writing scheme, which uses a continuous clock signal LP1, which is a component of LP, is divided into a

half cycle and then further divided into another half cycle. This clock signal LP can be construed as a pixel clock signal, therefore, LP1 is component of the pixel clock signal. The case of the full-screen display is not illustrated, but in the same manner as in the case of the partial display, polarity-switching for the liquid-crystal driving voltage is assumed to be performed every 3H. In this way, timing of polarity inversion of voltages applied to the liquid crystal in a display portion in the partial display can be arranged to be the same as that in the case of the full-screen display state. Therefore, it would be obvious that writing scheme that is applied to the partial display can also be applied to full screen writing scheme (paragraph 204). Also, partial and background display data is written into pixels of both areas of s rows and k rows of m columns (see claim 1), respectively. Claims 6, 15 and 24 are dependent on claims 1, 11, 20, respectively and are rejected on the same basis and what is stated above.

As pertaining to claim 7, Yamazaki teaches the transfer rate of row selection pulse is increased when the partial display instructions is issued and arrival of selections of rows (k) other than those rows of k that have already been detected (paragraph 146, 244). Claim 7 is dependent on claims 1 and 6 and is rejected on the same basis and what is stated above.

As pertaining to claims 30 and 38, Yamazaki discloses a partial display writing scheme, which uses a continuous clock signal LP1, which is a component of LP, is divided into a half cycle and then further divided into another half cycle. This clock signal LP can be construed as a pixel clock signal, therefore, LP1 is component of the pixel clock signal. Further, this can be construed as frequency divider because it is dividing the clock signal.

The case of the full-screen display is not illustrated, but in the same manner as in the case of the partial display, polarity-switching for the liquid-crystal driving voltage is assumed to be

performed every 3H. In this way, timing of polarity inversion of voltages applied to the liquid crystal in a display portion in the partial display can be arranged to be the same as that in the case of the full-screen display state. Therefore, it would be obvious that writing scheme that is applied to the partial display can also be applied to full screen writing scheme (paragraph 204). Also, partial and background display data is written into pixels of both areas of s rows and k rows of m columns, respectively (see claim 27). Claims 30 and 38 are dependent on claims 27 and 35, respectively and are rejected on the same basis and what is stated above.

As pertaining to claims 31 and 39, Yamazaki disclose a row clock controller for detecting an arrival of selection duration of rows other than the pixels of the area of k rows by m columns (paragraph 239) because the LCD must be able to detect which rows are being selected for writing or displaying of data, whether it is to the partial and/or background regions. Therefore, if it can detect the rows being selected it would be able to detect the rows not being selected. Claims 31 and 39 are dependent on claims 27, 30 and 35, 38, respectively and are rejected on the same basis and what is stated above.

4. Claims 28 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki as applied to claims 27 and 35 above, and further in view of Irwin (US 6,057,820).

As pertaining to claims 28 and 36, Yamazaki discloses what has previously been stated above. Furthermore, Yamazaki discloses a frame start signal FIRM so a one frame period to which one screen is scanned of a certain length (paragraph 158, 169, 203, 210, 243) and signal would also allow the detector to shift row to which the background display data is written based on the frame start signal (paragraph 158, 169, 203, 210, 243). Yamazaki does not disclose a

frame counter for counting frames. Irwin discloses an LCD Included in the timing and data signal source circuit 501 are a roll-over row counter 504 preferably receiving the HSYNC signal as input, and a roll-over frame counter 505 preferably receiving the VSYNC signal as input, so that the row counter 504 counts up to 512 rows as indicated by the HSYNC signal, then "rolls over" back to row one, and the frame counter 505 counts up to eight frames as indicated by the VSYNC signal, then "rolls over" back to frame one. The timing and data signal source circuit 501 generates the row address provided through row address lines 523 to the row decoder circuit 503 from an output of the row counter 504, and toggles the polarity modes of the video data provided to the column latches 501 and the front electrode voltage Vcom provided to the front electrode of the dot-matrix liquid crystal display in response to the frame counter 505 rolling over. In particular, each time the frame counter 505 rolls over, the polarity mode of the front electrode voltage Vcom is toggled after approximately one-half a refresh cycle delay (e.g., after the row counter 504 counts up to 256), so that the front electrode voltage Vcom is alternatingly in the 7.0 volts first polarity mode and the -2.0 volts second polarity mode for eight frames each. The timing and data signal source circuit 501 also toggles the polarity mode of the video data provided to the column latches 502 each time the frame counter 505 rolls over, so that the video data is alternatingly in the first polarity mode and the second polarity mode for eight frames each (col. 6, lines 28-54). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine the frame counter of Irwin with frame signal of Yamazaki. The suggestion/motivation for doing so would have been to provide a better display that is able function more efficiently when writing background data to a background display region and

partial data to a partial display region. Claims 28 and 36 are dependent on claims 27 and 35, respectively and are rejected on the same basis and what is stated above.

Response to Arguments

5. Applicant's arguments filed February 7, 2005 have been fully considered but they are not persuasive.

With respect to applicant's arguments of where Yamazaki fails to suggest where background display data is written into pixels and on page 20 of remarks, where in the present invention, pixels of a portion of the background display area are actively "selected" and "background display data is written". Examiner, respectfully, disagrees. As indicated in the previous office action, Yamazaki teaches two different driving methods for writing data into the partial and non-display regions frame by frame and into each active pixel. One method is MLS, multi-line scanning method, in which a group of lines are scanned (paragraph 31; 36; 167-168). The group can range from 2-7 lines. The second method is SA, smart addressing method, in which the lines are scanned one by one or it can be construed as a sequential scan method (paragraphs 31, 188-200). Yamazaki provides a driving method which comprises a function partially causing a display screen to be a display region, characterized in that selection voltages are applied in a selection period and non-selection voltages are applied in a non-selection period to the scanning electrodes, and where in a period other than the selection period, application voltages for all scanning electrodes are fixed, and application voltages for all the signal electrodes are fixed. As shown above, it is clear that Yamazaki teaches where data is *written* into *selected* pixels.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 703 306 5575. The examiner can normally be reached between 10:00 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (703) 306-0403. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Srilakshmi K. Kumar
Examiner
Art Unit 2675

SKK
February 18, 2005

Sumati Lefkowitz
SUMATI LEFKOWITZ
PRIMARY EXAMINER